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US-PAT-NO: 6366524

DOCUMENT-IDENTIFIER: US 6366524 B1

TITLE: Address decoding in multiple-bank memory architectures

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Abstract Text - ABTX (1):

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time, it is available to direct the

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US006366524B1

United States Patent
Abdelfattah

(10) Patent No.: US 6,366,524 B1
(43) Date of Patent: Apr. 2, 2002

ADDRESS DECODING IN MULTIPLE-BANK MEMORY ARCHITECTURES

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Assignee: Micron Technology Inc., Boise, ID (US)

Notice: Subject to any disclaimer the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 9 days.

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Filed: Jul. 26, 2000

Int. Cl. G11C 8/08
U.S. Cl. 365/230.04; 365/230.03; 365/230.08

Field of Search: 365/230.04, 230.03, 365/230.08, 185.11

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Primary Examiner—Huan Hoang
(74) Attorney, Agent, or Firm—Fogg Shier Polglaze LeBar & Jay, P.A.

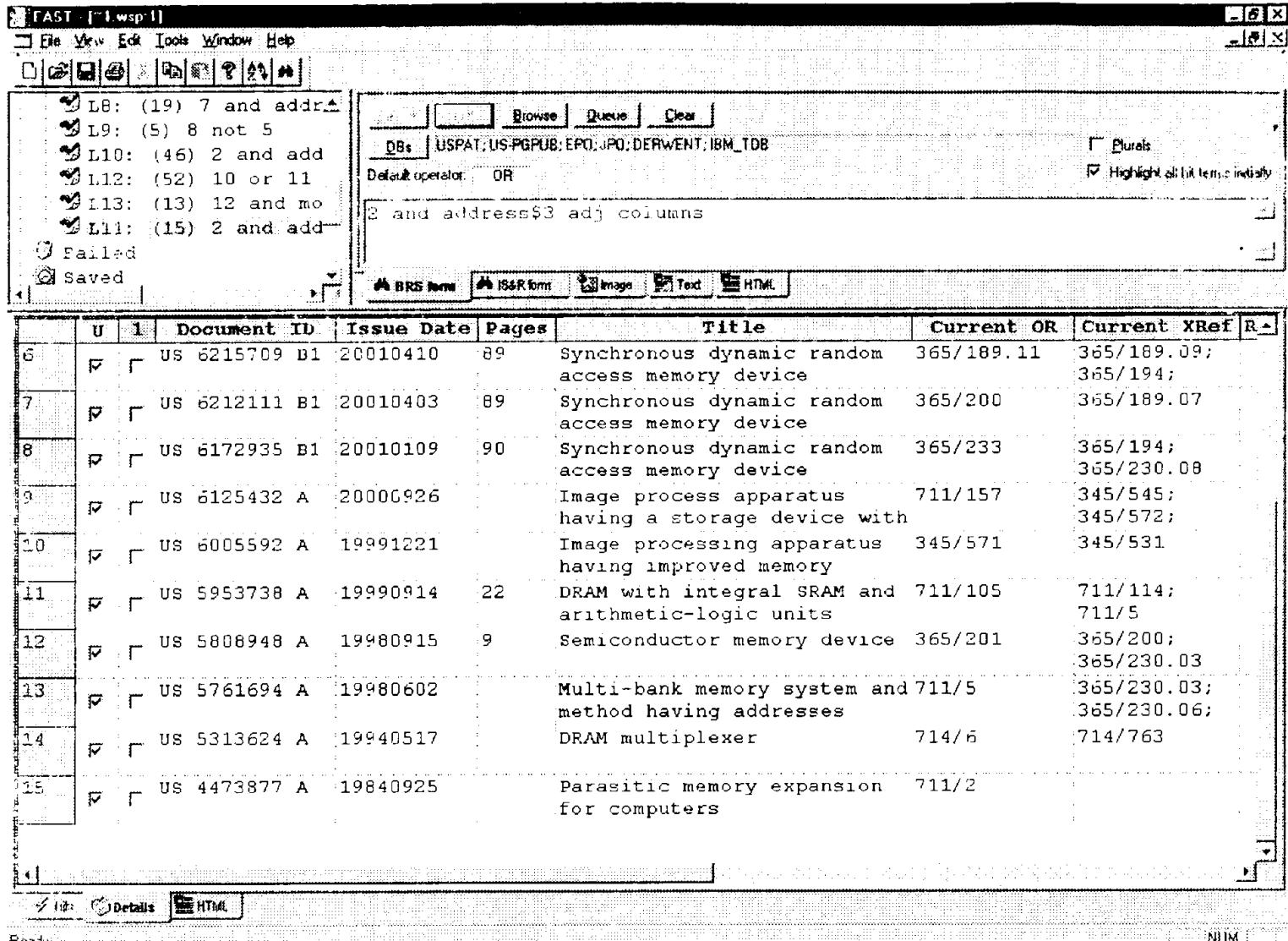
(57) **ABSTRACT**

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time, it is available to direct the second portion of the address to a proper decoder substantially without delay.

46 Claims, 8 Drawing Sheets

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L8: (19) 7 and add⁺
L9: (5) 8 not 5
L10: (46) 2 and add
L12: (52) 10 or 11
L13: (13) 12 and mo
L11: (15) 2 and add⁺
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1	P	US 20010050860	20011213	37	Non-volatile memory with background operation	365/185.11	
2	P	US 6373752	B1 20020416	88	Synchronous dynamic random access memory device	365/189.05	365/189.11; 365/230.06;
3	P	US 6351404	B1 20020226	88	Synchronous dynamic random access memory device	365/51	365/63
4	P	US 6333889	B1 20011225		Logic-merged semiconductor memory having high internal	365/230.03	365/51; 365/63;
5	P	US 6215726	B1 20010410	23	Semiconductor device with internal clock generating	365/233	327/141; 327/155;
6	P	US 6215709	B1 20010410	89	Synchronous dynamic random access memory device	365/189.11	365/189.09; 365/194;
7	P	US 6212111	B1 20010403	89	Synchronous dynamic random access memory device	365/200	365/189.07
8	P	US 6172935	B1 20010109	90	Synchronous dynamic random access memory device	365/233	365/194; 365/230.08
9	P	US 6125432	A 20000926		Image process apparatus having a storage device with	711/157	345/545; 345/572;
10	P	US 6005592	A 19991221		Image processing apparatus having improved memory	345/571	345/531
11	P	US 5953738	A 19990914	22	DRAM with integral SRAM and arithmetic-logic units	711/105	711/114; 711/5

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Find what mode

Find what: mode

Area: All Sel/Cur

Direction: Up Down

Match word: Whole word Part

Look in: Left Right

Look in: Grid Documents

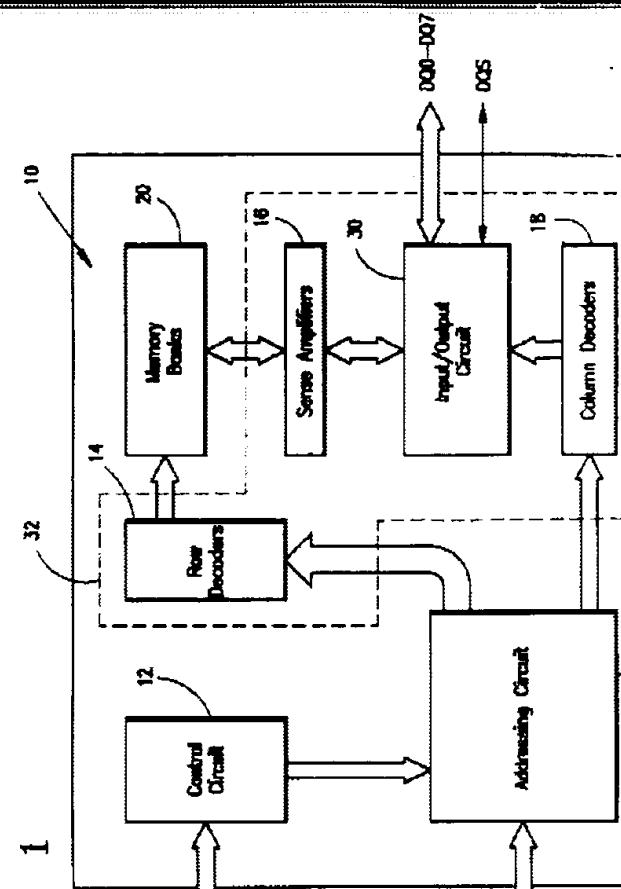
Match case

Find Next Cancel

rows in all of the banks 20 within the SDRAM 10. Examples of other well known commands include, but are not limited to, the ACTIVE, READ, WRITE, BURST TERMINATE, AUTO REFRESH, LOAD MODE REGISTER, COMMAND INHIBIT and NOP commands.

(13) The ACTIVE command is used to open up (or activate) a row of memory cells in a particular bank 20 for a subsequent access. The row remains active until a PRECHARGE command deactivates it. The READ command is used to initiate a burst read access for an active row. The WRITE command is used to initiate a burst write access for an active row. The READ and WRITE commands will also be accompanied with the column and bank addresses to complete the addressing for the command. The AUTO REFRESH command is used to refresh the contents of the memory arrays 20. The BURST TERMINATE command is used to truncate a read burst. The LOAD MODE REGISTER allows a mode register of the control circuit 12 to be loaded. The mode register contains information such as burst length and

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Courier New
12

[75] Inventor: Yoshihiko Okajima, Kawasaki, Japan
[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[11] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(c), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/792,134
[22] Filed: Jan. 31, 1997
[30] Foreign Application Priority Data
Feb. 2, 1996 [JP] Japan 6-017990
[51] Int. Cl. 7 G06F 12/00
[52] U.S. Cl. 711/169; 711/15; 711/164; 711/157
[56] Field of Search 711/14, 5, 105, 711/106, 111, 147, 148, 149, 150, 151, 152, 167, 166, 170, 173

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**Primary Examiner—Eddie P. Chan
Assistant Examiner—Kimberly McLean
Attorney, Agent, or Firm—Nikolic, Marushkin, Murray & Orr LLP**

[57] ABSTRACT

A memory system using at least one DRAM chip and equipped with an interface for transferring input/output data in a packet format includes a plurality of banks within each of the at least one DRAM chip. The memory system further includes a control circuit for accessing a bank for data transfer of a given packet when the bank is different from a previous bank accessed for an immediately preceding packet, and for waiting for an operation to complete in the bank when the bank is the same as the previous bank.

6 Claims, 17 Drawing Sheets

<img alt="Detailed block diagram of a memory system architecture. The diagram shows various components connected via buses and control signals. Key components include an INPUT-DIGITAL BUFFER, ADDRESS DECODER, WORD LINE DRIVER, LOCAL ROW SCHEDULER, GLOBAL ROW SCHEDULER, COLUMN ADDRESS REGISTER, READWRITE MODE SELECT, INTERNAL CLOCK GENERATOR, CONTROL SIGNAL BUFFER, and a BURST ADDRESS REGISTER. Signal paths are labeled with numbers such as 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 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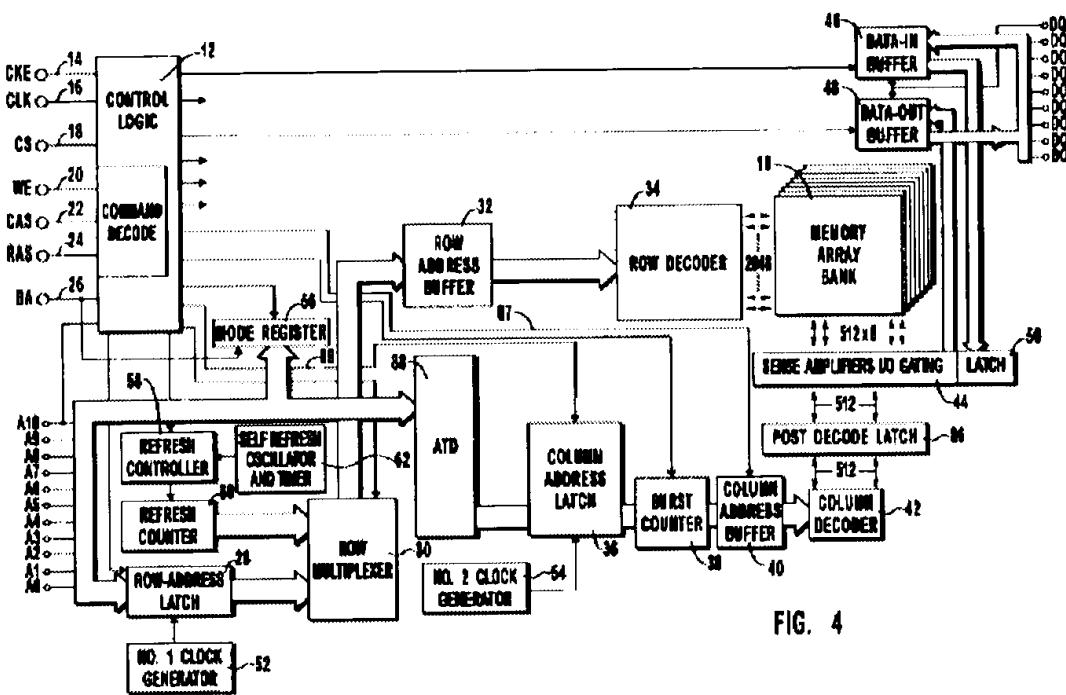


FIG. 4

Details

Text

Image

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Full

Ready

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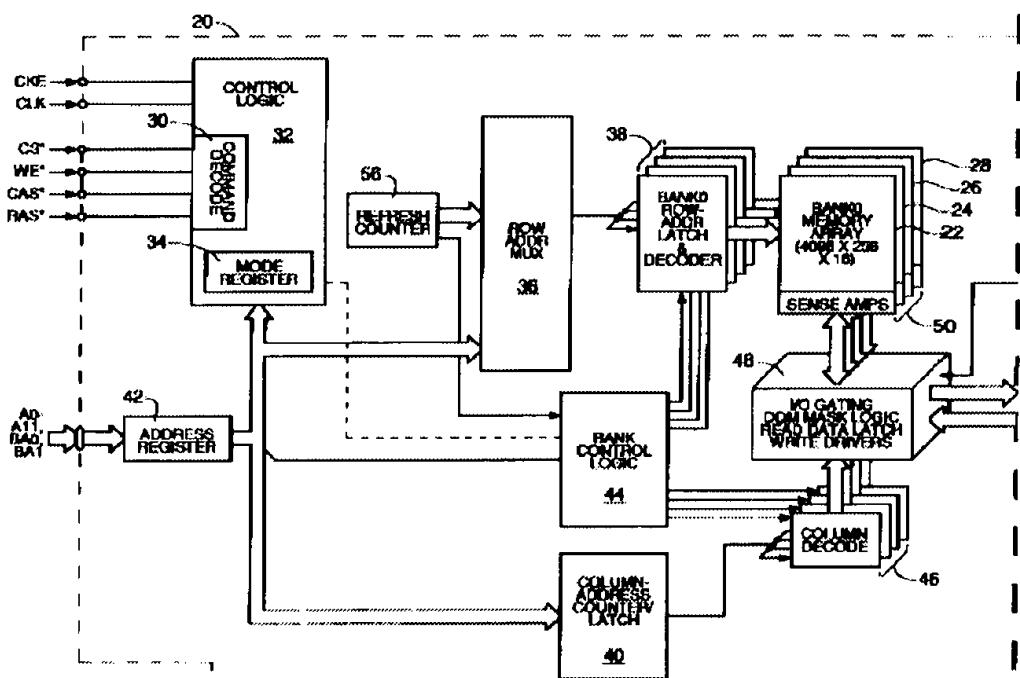


FIG. 1A

FIGURE 1B

